

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

REMARKS

Following the foregoing amendment, Claim 1 is pending in the application. Claim 1 has been amended. No new matter has been added by the amendment. Reconsideration and allowance of the application, as amended, are respectfully requested.

Objection to the Title

The Examiner states that a more descriptive title is required that is clearly indicative of the invention to which the claims are directed. Applicants have amended the title, and submit that the title, as amended, is clearly indicative of the invention to which the claims are directed.

35 U.S.C. §112 Indefinite Rejection of Claim 1

The Examiner has rejected Claim 1 under 35 U.S.C. § 112, first paragraph, stating that Claim 1 is not supported by the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Specifically, the Examiner states that the written description never discloses the polycrystalline silicon film being formed by irradiating a laser beam on a surface of an amorphous silicon film to heat the amorphous silicon film. Applicants submit that the phrase “the polycrystalline silicon film being formed by irradiating a laser beam on a surface of an amorphous silicon film to heat the amorphous silicon film” is supported on page 5, lines 29-31 of the present specification. Furthermore, Applicants have amended Claim 1 such that the phrase “the laser beam is scanned on the surface of the amorphous silicon film such that laser energy

*Application No. 09/730,875*

increases in order of the substrate, one of the pair of tapered end portions, and the center portion” is changed to the phrase “the laser beam is scanned on the surface of the amorphous silicon film such that a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than a second portion of the amorphous silicon film above the insulator substrate and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions” on the basis of the description of page 6, lines 17 to 31 of the present specification.

The Examiner has also rejected Claim 1 under 35 U.S.C. § 112, first paragraph, stating that the written description never discloses how a uniform grain size of the polycrystalline silicon film is acquired by securing a gate withstand voltage of the thin film transistor and preventing the inclined surfaces of the pair of tapered end portions from increasing. However, the present specification discloses that:

An angle greater than  $40^{\circ}$  reduces the coverage of the gate i insulator film 80 to lower the gate withstand voltage. An angel smaller than  $5^{\circ}$  means an increased surface of the tapered portion 76b, which causes a variation in the membranous of the polycrystalline silicon film 81.

Since the above disclosure can be interpreted as defining an angle of each of the pairs of tapered end portions within a rage of  $5^{\circ}$  to  $40^{\circ}$  to secure a gate withstand voltage and prevent the

*Application No. 09/730,875*

inclined surfaces of the pair of tapered end portions from increasing, a uniform grain size of the polycrystalline silicon film is acquired.

35 U.S.C. §103(a) Obviousness Rejection of Claim 1

The Examiner has rejected Claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Tsai et al. in view of Ono et al. The present invention is directed to a bottom gate type TFT having a gate electrode having a pair of tapered end portions within a range of 5° to 40° in order to acquire a uniform grain size of the polycrystalline silicon film above the center portion and the pair of tapered end portions of the gate electrode.

Tsai et al. (U.S. Patent No. 5,892,246) is directed to a polysilicon TFT formed by a laser annealing step to cause an amorphous silicon layer to crystallize into polysilicon. However, Tsai et al. does not disclose that a gate electrode includes a pair of tapered end portions each having an angle within a range of 5° to 40° so that a uniform grain size of the polycrystalline silicon film is acquired above the center portion and the pair of tapered end portions.

Ono et al. (U.S. Patent No. 5,760,854) is directed to a liquid crystal display apparatus including a gate electrode (2) having an end portion shaped in a taper of 6° to 10° in order to decrease a probability of causing crack at the overriding portion of a gate insulating layer (4) comprised of a silicon nitride film (column 18, lines 7-11). However, Ono et al. does not teach or suggest setting the taper angle of the end portion within 5° to 40° in order to acquire a uniform grain size of the polycrystalline silicon film is acquired above the center portion and the pair of tapered end portions. Furthermore, Ono et al. does not teach or suggest scanning the lower beam on the surface of the amorphous silicon film such that a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than

Application No. 09/730,875

a second portion of the amorphous silicon film above the insulator substrate and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions.

Accordingly, Applicants submit that the present invention, as claimed by Claim 1, is not obvious by the combination of Tsai et al. and Ono et al.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version With Markings to Show Changes Made."**

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

SHERIDAN ROSS P.C.

By: Kenneth C. Winterton

Kenneth C. Winterton  
Registration No. 48,040  
1560 Broadway, Suite 1200  
Denver, Colorado 80202-5141  
(303) 863-9700

Date: April 24, 2002

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE TITLE:**

The title of the invention has been amended as follows:

THIN FILM TRANSISTOR [AND METHOD OF FABRICATING THE SAME] WITH  
GATE ELECTRODE HAVING TAPERED END PORTIONS"

**IN THE CLAIMS:**

Claim 1 has been amended as follows:

1. (Once Amended) thing film transistor comprising:

an insulator substrate;

a gate electrode located on the insulator substrate;

a gate insulator film provided above the insulator substrate an the gate electrode; and

a polycrystalline silicon film located on the gate insulator film, the polycrystalline silicon film being formed by irradiating a laser beam on a surface of an amorphous silicon film to heat the amorphous silicon film,

the gate electrode having a center portion with a flat surface and a pair of tapered end portions with inclined surfaces, an angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 5° to 40° so that a uniform grain size of the polycrystalline silicon film is acquired [by securing] above the center portion and the pair of tapered end portions, a gate withstand voltage of the thin film transistor, and [preventing] the inclined surfaces of the pair of tapered end portions are prevented from increasing, wherein the laser beam is scanned on the surface of the amorphous silicon film such that [laser energy increases in order of the substrate, one of the pair of tapered end portions,

*Application No. 09/730,875*

and the center portion] a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than a second portion of the amorphous silicon film above the insulator substrate, and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions.